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A Design of A Novel ALU Architecture using Reversible Logic Technique

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Abstract: Reversible Logic has come up with an significant feature of a no defiance of power and has become most standard technique in design of high efficiency Microprocessor. ALU is a core of processors that accomplishes arithmetic and logical operations, But the design of ALU is an undertaking task for the design researchers. From the analysis of literature survey, the past reversible ALU were designed each design have their advantages and limitations such as fixed or limited number of operations and more garbage output lines. In this paper we have been tried to add many ALU operations such as Eight Arithmetic operation Seven logical along with Shift, Vedic Multiplication and Comparison operations so all these 21 operations are carried out on 2-bit ALU and implemented in different modules and all these modules are built with reversible gates and integrated or incorporated on unique design and these different operations are carried out based on select lines. This design is executed in VHDL(Verilog Hardware Description Language) programming language and simulation and synthesis is done with use of Xilinx ISE 14.7 simulation Tool.

Keywords: ALU, Basic Reversible Logic gates, Reversible ALU.

I. INTRODUCTION

In past VLSI industry the manufacturing of chip was quite demanding in high power dissipation to circumference of circumstances (environment)which causes harm to devices. Hence over whelmed reversible logic being to avoid problem of power dissipation. Reversible logic achieves zero power loss so regular traditional designs are made as reversible by the use of basic reversible gates replacing the irreversible logic gates.

In 1961 Laundauer invented new proposal for the conventional circuits that effects information loss and this states that " At room temperature, every bit operation causes Kt*log2 joules of heat energy loss. Where K is $1.38*10^{23}$m(joules/kelvin) Boltzmann's constant factor, t is absolute ideal temperature. In 1973 Bennett suggested irreversible circuits must be replaced with reversible circuits to prevent loss of bits during estimation of process. This statement achieves better results in design of circuits that indirectly helps to improve the consistency of chip. ALU is a control unit of microprocessors that implements both arithmetic and logical functions. ALU has been designed in traditional way but this approach produces more power loss. Later this ALU is designed in reversible way no power loss but yet much effort to be achieve because earlier systems will perform few operations. This motivates the design of reversible ALU that performs more operations and reduces delay of the design. So in this work reversible ALU perform 21 functions based on five S0,S1,S2,S3,S4,S5 select lines. In this paper 2-bit reversible ALU has been proposed with all 21 operations on single platform and simulation is on Xilinx 14.7 tool.

II.BASICS OF REVERSIBLE LOGIC

In accomplishment of gates are AND,NAND,OR, NOR, NOT gates are basically irreversible in nature with an unequal number of inputs and outputs causes loss of power in systems.

According to C.H. Ben net there are many of the systems are designed with reversible gates with use of Fredkin, Peres and HNG gates and other gates are discussed next section.

The basic principle of reversible logic is an Bijective this implies that same number of inputs i.e. one-one mapping that relates inputs can be obtained from output *and vice-versa.

The universal common structure of an reversible gate has 'm' inputs and 'm' outputs (m*m)circuit. But in traditional designs the number of outputs are less than inputs where as seen from below figure reversible gate has equal numbers.

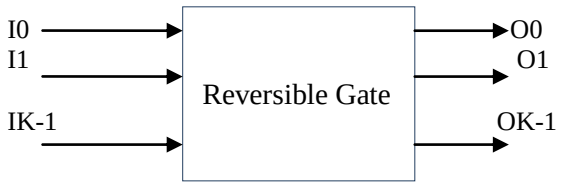

Figure 1: General Block Diagram of Reversible Gate

Due to mapping of input and output no power loss and these designs would enhance the portability of device so there are wide applications are Nano Circuits, and quantum designs, Bio application field and hand held devices.

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III. DESIGN OF REVERSIBLE ALU WITH FOLLOWING BASIC REVERSIBLE GATES

Currently the implementation of many reversible gates becoming an greater approach. some of the exciting the most basic reversible gates are usually known as QUBIT gates each of them are explained below.

➢ NOT GATE

The Not gate has 1*1 vector of input and output and its quantum cost is 1.

Figure 2: NOT Gate

➢ FEYNMAN GATE

This is of 2*2 Feynman gate it has quantum cost is 2,this gate is mainly used for replication of the output. The two binary inputs A,B and outputs C,D are defined below.

P=A
Q=A XOR B

Figure 3: Feynman Gate

➢ TOFFOLI GATE

The Toffoli gate or Doubly controlled Not(CNOT) and this is a3*3 universal reversible gate with higher quantum cost of 5. As shown in below figure this gate has three inputs and three outputs, the first output is same as first input and other outputs are expressed below.

P=A
Q=B
R=AB XOR C

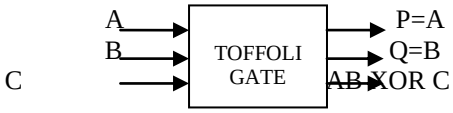

Figure 4: Toffoli Gate

➢ FREDKIN GATE

The Fredkin gate is known as controlled swap gate. This is 3*3 universal gate. A,B,C are inputs and P,Q, Rare equivalent outputs. The first input is appeared as first input and other two inputs are get swapped hence the name of this gate as swap gate.

P=A
Q=A'B+AC
R=AB+A'C

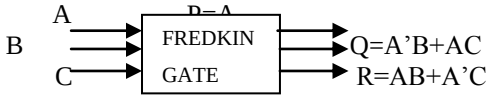

Figure 5:Fredkin Gate

A. Advanced Reversible Gates

❖ NEW GATE

The most advanced new gate has 3*3 input vector(A,B,C) and relating output vector(P,Q,R) are defined by following equation.

P=A
Q=AB XOR C
R=B' XOR A'C

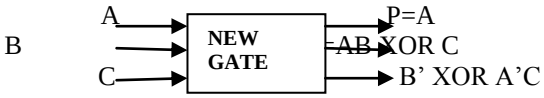

Figure 6: New Gate

➢ PAOG(PERES AND-OR)GATE

The PAOG gate is an 4*4 novel programmable reversible gate. As name itself indicates this is an extended form of Peres gate and applied in ALU realization. A,B,C,D are inputs to gate and P,Q,R,S are equivalent outputs. The basic OR, NOR, AND,NAND logical operations can be performed by this PAOG gate.

P=A
Q=A XOR B
R=AB XOR C
S=((A XOR B)XOR D)XOR(AB XOR C)

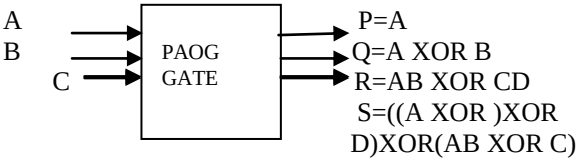

Figure 7: PAOG Gate

➢ TR GATE

The next advanced TR gate has 3*3 input vector(A,B,C) and corresponding output vector(P,Q,R) are defined below. This gate is widely used in subtractor circuit design.

P=A
Q=A XOR B
R=AB'XOR C

Figure 8: TR Gate

➢ BJN GATE

This is also a 3*3 advanced reversible gate and used in comparator circuit design. The inputs A,B,C and corresponding outputs P,Q,R are illustrated in below figure.

P=A
Q=B
R=(A+B)XOR C

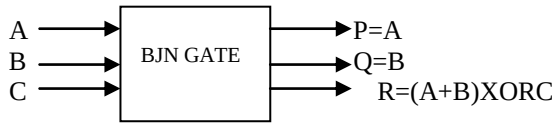

Figure9: BJN Gate

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IV. LITERATURE SURVEY

We have analyzed the literature survey of existing reversible ALU many of researchers have provided significant contributions in reversible ALU design but each have some benefits and limitations. So still much effort must be provide so some of the existing designs are explained below. Akanksha Dixit, Vionodkapseet.al[1]has described the design of ALU based control unit has for the parallel adder. In this paper low quantum cost has achieved by using D Peres gates. Based on three control signal performs 12 arithmetic and logical operations. this design has 10 gate count,8 garbage output,29 quantum constant 4 constant inputs less compared to existing systems.

ShubhanginiUgale,VipinSBhureet. al[2] has described the design of 16-bit reversible ALU performs four arithmetic operations and four logical operations such as AND,NAND,NOT and XOR. Since this is an reversible ALU design and power is less because it uses Feynman and Fredkin gate and each sub modules are integrated and desired output is obtained based on select lines. The disadvantage is that in ALU the divider reversible block has not been implemented.

Prasanth.R.Yelekar,Sujata.S.Chiwande,et.al[3]has described the combinational and sequential circuits design, also gives build of an adder circuit using reversible gates such as Peres gate and TSG gates. In this paper have been D-Latch and using SaymanGate, also Feynman gate used to copy output of SG gate,T-Flipflop using Fredkin and Feynman gates. one more design 4-bit Asynchronous Up/Down counter has designed based on control signal it performs either up/down count operation. AnkitaVerrma,RitaJain,et.al[4]has described design of Adder/Subtractor and Multiplier modules are Indi dually implemented with use of 4*4 DKG Gate that act as adder/subtractor based on control signal either 0 or 1.the decoder logic acts as selection unit so used to select one of the operation while other modules are deactivated thus this reduces the gate count from 40% to 30%.the operations are implemented from this design.

V. PROPOSED DESIGN METHODOLOGY &IMPLEMENTATION

The realization of ALU can be achieved with use of reversible gates such as Peres gate, Fredkin gate and TR gate and BJN gates etc. the ALU is different for different computers but the design of AU unit is quite similar and difficult. The arithmetic and logical unit are main component of ALU those operations are realized with make use of reversible gates that are places an role in avoid of energy loss.

The earlier designs are analyzed and compared in terms of gate count, garbage outputs, quantum cost and number of operations performed by the proposed designs. In our design 21 operations are based on multiplexer as shown in figure.

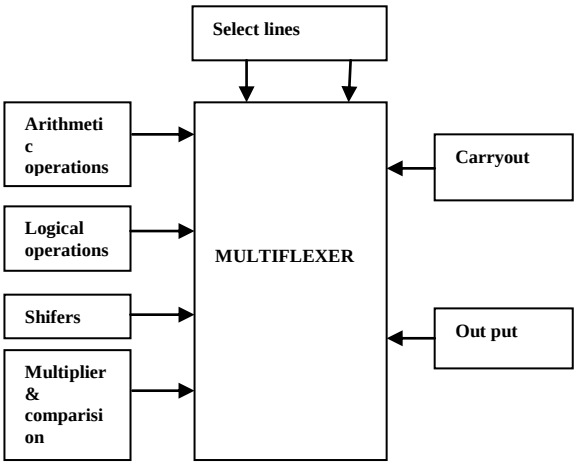

Figure 10: Proposed Reversible ALU Architecture

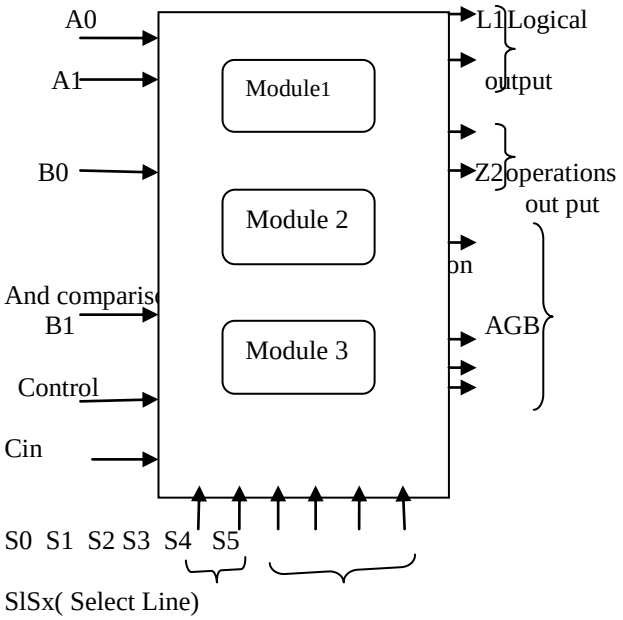

Figure 11:View of Proposed Diagram

A. PROPOSED DESIGN DESCRIPTION

The implementation part our design is categorized into three sub modules.

- first module accomplishes ten logical operations such as

1.OR 2.NOR 3.AND 4.NAND 5.XOR 6.NOT 7.XOR 8.NOT 9.Transfer (A or B) 10.Shift(Left or Right).

- Second module accomplishes seven arithmetic operations such

11. Adddition 12.Subtractin 13.Addition with carry 14.Subtraction with Borrow 15.Increment 16.Decrement 17.Complement

- Third module accomplishes two operations such as

18. Vedic Multiplier
19. Comparison

I. A>B

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II. A<B
III. A=B

The above three modules are combined in a main module as illustrated in above figure 11. Here the five select lines are used implement the 21 operations. In our design we have proposed 2-bit reversible ALU with new Architecture.

VI. SIMULATION RESULTS

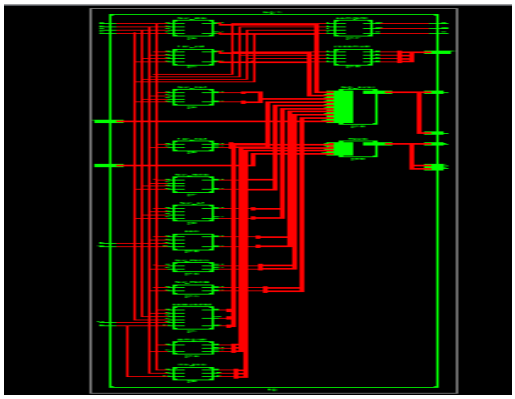

Figure 12.RTL(Register transfer Logic) View of Reversible ALU

The simulation results are shown in Figure 13.TheTop module has A,B are 2-bit inputs as A0,A1,BO,B1 with Control, Cin are act as control signals ,the extra two control signal Left, Right signals to control left/right shift operation and five select lines are S0,S1,S2,S3,S4,S5. All these control helps to perform 21 ALU operations and particular output for each operation. Based on referring the following truth table.

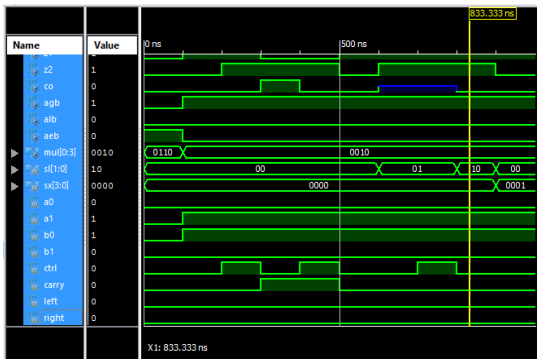

Figure 13: Simulation Output with Test Bench Waveform

S0	S1	S2	S3	ALU Operations
0	0	0	0	AND
0	0	0	1	XOR
0	0	1	0	NOR
0	0	0	1	NOT
0	0	1	0	NAND
0	0	1	1	OR
0	1	0	0	SHIFT(LEFT/RIGHT)
0	1	0	1	TRANSFER A
0	1	1	0	TRANSFER B

S4	S5	Control	Cin	ALU Operations
0	0	0	0	ADDITION
0	0	0	1	ADDITION WITH CARRY
0	0	1	0	SUBTRACTION
0	0	1	1	SUBTRACTION WITH CARRY
0	1	0	0	INCREMENT
0	1	1	0	DECREMENT
1	0	0	0	COMPLEMENT

VII. DEVICE UTILIZATION SUMMARY (ESTIMATED VALUE)

This summary is generated by synthesis tool. This will gives ratios of number of slices,,input-output functions are internally utilized helps to analyzed the gate count(number of gates used).

Device Utilization Summary (estimated values)			
Logic Utilization	Used	Available	Utilization
Number of Slices	15	3584	0%
Number of 4 input LUTs	28	7168	0%
Number of bonded IOBs	26	97	26%

Figure 14: Device Utilization Summary

VIII. DELAY ANALYSIS

The simulation tool itself generates the delay and timing details of the design. This details is the delay induced between the path from data signal (a0) to output signal(aeb)is 8.089ns(6.103ns logic,1.98ns route)is lees seen from other designs.

```
==========================================================================
Timing constraint: Default path analysis
  Total number of paths / destination ports: 18 / 6
--------------------------------------------------------------------------
Delay:               8.089ns (Levels of Logic = 3)
  Source:            a0 (PAD)
  Destination:       aeb (PAD)

  Data Path: a0 to aeb
                                Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     IBUF:I->O             15   0.715   1.305  a0_IBUF (a0_IBUF)
     LUT2:I0->O             1   0.479   0.681  g18/g1/w41 (g18/g1/Mxor_r_Resul
     OBUF:I->O                  4.909          mul_0_OBUF (mul<0>)
    ----------------------------------------
    Total                      8.089ns (6.103ns logic, 1.986ns route)
                                       (75.5% logic, 24.5% route)

==========================================================================
```

Figure 15:Timing Details

IX. APPLICATIONS

Reversible designs have advantages in many of Fields. such as

- Nanotechnology and computing Devices.
- In DSP(Digital Signal Processing) Applications..

- DNA computing and Bio Information.
- Ultra low Power VLSI Circuits.
- In design of Adders and Comparators.
- In design of Combinational circuit(Full Adder) and Sequential circuit(Latches, Flip flop and Asynchronous design).

X. CONCLUSION&FUTURE WORK

The Reversible ALU performs different Arithmetic and Logical operations. But many of the designs performs five or six fixed number of operations and these operations are varied from one design to other design this design differs from earlier design in number of operations.
The scope behind this work is that all different 21 operations mentioned above can be implemented in single design on 2-bit ALU with an reduced delay. This design simulated on Xilinx ISE 14.7 and synthesized using model sim Altera Quartus II 6.6d tool.

The Future work can be made the other operations can be designed with use of this same architecture, this architecture can be further improved to make use towards progress in design of reversible logic based design in order to achieve better performance with zero power loss.
Here 2-bit reversible ALU can be enhanced to Higher bits of Arithmetic and logical operations.

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BIOGRAPHIES

SHRIDEVI BIRADA Rshe has received her Bachelor of Enginneering in Electronics and communication engineering in Proudhadevaraya Institute of Technology(P.D.I.T) at Hospet and currently she is pursing(Final Year) M.Tech in VLSI Design and Embedded System in Department of Electronics & Communication Engineering, at Ballari Institute of Technology and Management(B.I.T.M), Bellary, India. She is currently working on a project tilled as " A Design of A Novel ALU Architecture using Reversible Logic Technique" as a parcial fullfillment for her M.Tech Engineering Degree.

NILAM C she had received her Bachelor of Engineering in Electronics & Communication Engineering, and M.Tech in Computer Network Engineering, and currently she is working as a Assistant Professor in Electronics& Communication Department in Ballari Institute of Technology and Management(B.I.T.M), Bellary, and she is Pursing PhD and her domain of interest or current research in Communication field.